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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,666	01/22/2004	Carlos Dangelo	NANOC002NP	5164

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/762,666	DANGELO, CARLOS	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 28-32* is/are pending in the application.

4a) Of the above claim(s) *1-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-26 and 28-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05-23-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 22 and 24-26 are rejected under 35 U.S.C. 102(a) as being anticipated by Hasegawa et al. (US Pat. 6452274).

Regarding claim 22, 24, 25, Hasegawa et al. disclose an integrated circuit structure (ICS)/device (see Fig. 7F) comprising a heat conducting structure/device, the ICS comprising:

- a heat conductive network (see 67/77 in Fig. 7F; Col. 21, lines 32-38) extending from a top surface of an active device layer (see top surface of 62 in Fig. 7F), through a plurality of wiring/interconnect levels (72/82 in Fig. 7F), to a top surface of the ICS
- the heat conductive network comprising a plurality of heat conductive dummy vias/plugs (67/77 in Fig. 7F; Col. 18, line 47) traversing the wiring/interconnect levels (see Fig. 7F), the vias/plugs comprising tungsten (Col. 18, line 47) and being oriented in a direct line from the top surface of the active device layer to that of the ICS (see Fig. 7F)

- the heat conductive vias/plugs being electrically isolated from metal conductors of the wiring/interconnect levels (see 67/77 and 66/71/76 in Fig. 7F), and
- heat generated by active devices in the device layer being conducted through the heat conductive network to the top surface of the ICS (Col. 21, lines 32-38)

(Fig. 7F; Fig. 6A-7F; Col. 18, line 20- Col. 21, line 46).

Regarding claim 26, Hasegawa et al. disclose the entire claimed structure as applied to claim 22 above, wherein Hasegawa et al. disclose each via/plug traversing a single level of wiring/interconnect metal level (see 72 in Fig. 7F) wherein the single level of wiring interconnect level being over a single layer of intermetal insulating/dielectric layer (64 in Fig. 1; Col. 18).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (US Pat. 6452274) in view of Awano (US Pat. Application Pub. 2002/0163079).

Regarding claim 23, Hasegawa et al. disclose the entire claimed structure as applied to claim 22 above, except the heat conductive vias comprising carbon nanotubes.

Awano teach heat dissipating contact structure comprising heat conductive vias (see 36/37 in Fig. 4) where the vias comprise carbon nanotubes to provide improved heat dissipation (sections 0085-0087 and 0071-0086).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the heat conductive vias comprising carbon nanotubes as taught by Awano so that the thermal conduction and heat dissipation can be improved in Hasegawa et al's ICS.

5. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dahl et al. (US Pat. Application Pub. 2002/0130407) in view of Cromwell (US Pat. 5926370).

Regarding claim 28, Dahl et al. disclose an integrated circuit (IC) chip substrate/die having enhanced power dissipation and improved heat transfer structure (see 601 in Fig. 6C), the IC chip/die comprising:

- a substrate having a top surface upon which power generating devices of the IC are fabricated (see sections 0116 and 0136; Fig. 6 and 9) and a back/bottom surface essentially parallel to the top surface
- a plurality of cavities/holes (see 633/634 in Fig. 6C) extending a predetermined distance from the bottom surface to the top surface, the predetermined distance being less than the distance between the top and bottom surfaces, the cavities/holes being filled with heat conductive media (HCM) in a form of heat conducting conduits or heat pipe including highly thermally conductive medium comprising a variety of diamond containing material (sections 0007 and 0118-0122) and the cavities/holes being distributed/located directly below the IC devices/power generating devices of the substrate to provide the heat removal from the desired areas of the substrate (see Fig. 6C)
- the HCM having thermal conductivity greater than the substrate/silicon, and
- the heat produced by the IC devices/power generating devices being transferred to the back/bottom surface via the HCM

(Fig. 6C; sections 00116-0122).

Dahl et al. fail to teach the HCM comprising copper.

Cromwell teaches a heat dissipation/heat sink structure using conventional heat pipes (31 in Fig. 4b) where the heat pipes are made of conventional metal such as copper (Col. 10, line 22; Col. 9 and 10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the HCM comprising copper as taught by Cromwell so that the fabrication and processing can be simplified in Dahl et al's IC cooling structure.

6. Claims 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dahl et al. (US Pat. Application Pub. 2002/0130407) in view of Montgomery et al. (US Pat. Application Pub. 2003/0117770).

Regarding claims 29 and 30, Dahl et al. disclose an integrated circuit (IC) chip substrate/die having enhanced power dissipation and improved heat transfer structure (see 601 in Fig. 6C), the IC chip/die comprising:

- a substrate having a top surface upon which power generating devices of the IC are fabricated (see sections 0116 and 0136; Fig. 6 and 9) and a back/bottom surface essentially parallel to the top surface
- a plurality of cavities/holes (see 633/634 in Fig. 6C) extending a predetermined distance from the bottom surface to the top surface, the predetermined distance being less than the distance between the top and

bottom surfaces, the cavities/holes being filled with heat conductive media (HCM) in a form of heat conducting conduits or rods including highly thermally conductive medium comprising a variety of diamond containing material (sections 0007 and 0118-0122) and the cavities/holes being distributed/located directly below the IC devices/power generating devices of the substrate to provide the heat removal from the desired areas of the substrate (see Fig. 6C)

- the HCM having thermal conductivity greater than the substrate/silicon, and
- the heat produced by the IC devices/power generating devices being transferred to the back/bottom surface via the HCM

(Fig. 6C; sections 00116-0122).

Dahl et al. fail to teach the HCM comprising carbon nanotubes.

Montgomery et al. teach a thermal interface structure (TIS)/heat dissipation structure wherein the HCM comprises heat conducting rods in form of carbon nanotubes (see 26 in Fig. 4) to provide improved thermal conductivity and heat dissipation between a die and a heat sink for the TIS (section 0017; pp. 1 and 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the HCM comprising carbon nanotubes as taught by Montgomery et al. so that the thermal conduction and heat dissipation can be improved in Dahl et al's IC.

Regarding claims 31 and 32, Dahl et al. and Montgomery et al. teach the entire claimed structure as applied to claims 29 and 30 above, wherein Dahl et al. teach the IC devices/power generating devices comprising transistors having source/drain regions (see 902 in Fig. 9; section 0136), such device configuration in the IC package having the plurality of cavities/HCM being distributed/located along the bottom surface of the substrate (see Fig. 6C) provides the cavities/HCM directly below respective source, drain and isolation regions.

Response to Arguments

7. Applicant's arguments with respect to claims 22-6 and 28-32 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steven Loke can be reached on 571-272-1657.
The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

08-26-05

NITIN PAREKH

PRIMARY EXAMINER

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